What is claimed is:

1. A method for forming an electrical interconnect, comprising the following steps:

a) creating a first electrically conductive layer overlying a substrate and having an opening therein exposing a portion of the substrate;

b) creating a second electrically conductive layer to overlie said first electrically conductive layer and the substrate, said second electrically conductive layer electrically contacting the substrate in the portion of the substrate which was exposed; and

c) removing said second electrically conductive layer from overlying said first electrically conductive layer, a portion of said second electrically conductive layer remaining in electrical contact with the portion of the substrate which was exposed.

2. A method for forming an electrical interconnect, comprising the following steps:

a) creating a first electrically conductive layer overlying a substrate;

b) patterning said first electrically conductive layer to create a masked region and an unmasked region;

c) exposing the substrate in said unmasked region, thereby forming a via in said first electrically conductive layer;

d) creating a second electrically conductive layer to overlie said first electrically conductive layer and the substrate, said second electrically conductive layer electrically contacting the substrate in the unmasked region; and

e) removing said second electrically conductive layer from overlying said first electrically conductive layer, a portion of said second electrically conductive

layer remaining in the via and contacting the substrate to form the electrical interconnect.

3. A method for forming an electrical interconnect, comprising the following steps:

a) creating a first electrically conductive layer overlying a substrate;

b) patterning said first electrically conductive layer to create a masked region and an unmasked region;

c) exposing the substrate in said unmasked region, thereby forming a via in said first electrically conductive layer;

d) creating a second electrically conductive layer to overlie said first electrically conductive layer and the substrate, said second electrically conductive layer electrically contacting the substrate in the unmasked region;

e) removing said second electrically conductive layer from overlying said first electrically conductive layer, a portion of said second electrically conductive layer remaining in the via and contacting the substrate to an electrical plug, the electrical plug and the first electrically conductive layer forming the electrical interconnect; and

f) retaining a portion of said first electrically conductive layer during said step of removing.

4. The method as specified in Claim 3, defining a height of the electrical plug by a height of said first electrically conductive layer remaining subsequent to said step of removing, such that the height of the electrical plug is equal to the height of said first electrically conductive layer.

5. The method as specified in Claim 3, further comprising the following steps:

a) creating an etch stop layer overlying said first electrically conductive layer prior to said step of exposing, the via thereby formed in said first electrically conductive layer and said etch stop layer; and

b) defining a maximum height of the electrical plug by a total height of said first electrically conductive layer and said etch stop layer, such that the height of the electrical plug is equal to or less than the total height of said first electrically conductive layer and said etch stop layer.

6. The method as specified in Claim 5, wherein said step of exposing comprises etching said first electrically conductive layer and said etch stop layer.

7. The method as specified in Claim 5, wherein said step of removing comprises etching said second electrically conductive layer, said etch stop layer protecting said first electrically conductive layer during said step of removing.

8. The method as specified in Claim 3, wherein said step of removing comprises performing a chemical mechanical planarization of said second electrically conductive layer to expose said first electrically conductive layer.

9. The method as specified in Claim 3, wherein said step of removing comprises etching said second electrically conductive layer.

10. The method as specified in Claim 3, further comprising the following steps:

a) protecting at least said second electrically conductive layer with a photoresist mask; and

b) removing exposed portions of said first electrically conductive layer, remaining portions of said first electrically conductive layer vertically and electrically contacting the electrical plug.

11. The method as specified in Claim 10, further comprising the step of creating a protective layer overlying said second electrically conductive layer remaining subsequent to said step of removing said second electrically conductive layer, said

protective layer protecting said second electrically conductive layer during said step of removing exposed portions of said first electrically conductive layer.

12. The method as specified in Claim 3, further comprising the following steps:

a) creating a first etch stop layer overlying said first electrically conductive layer prior to said step of exposing;

b) creating a layer which is capable of reacting with said second electrically conductive layer to form a layer irresponsive to an etchant which is capable of etching said second electrically conductive layer, said layer which is capable of reacting with said second electrically conductive layer overlying said first etch stop layer and said the electrical plug;

c) creating a reaction between said layer which is capable of reacting with said second electrically conductive layer and the electrical plug to form a second etch stop layer overlying the electrical plug, said first etch stop layer protecting said first electrically conductive layer from reacting with said layer which is capable of reacting with said second electrically conductive layer during said step of creating said reaction;

d) removing unreacted portions of said layer which is capable of reacting with said second electrically conductive layer;

e) removing at least portions of said first etch stop layer while retaining said second etch stop layer;

f) removing at least portions of said first electrically conductive layer to further define a shape of the electrical interconnect; and

g) retaining the electrical plug in its entirety during said steps (e and f of Claim 12) of removing.

13. The method as specified in Claim 3, further comprising doping said first and said second electrically conductive layers to increase a conductivity thereof.

14. The method as specified in Claim 3, further comprising the step of using silicon as said first and said second electrically conductive layers.

15. A method for forming an electrical interconnect, comprising the following steps:

a) creating a first electrically conductive layer overlying a substrate;

b) patterning said first electrically conductive layer to create a masked region and an unmasked region;

c) exposing the substrate in said unmasked region;

d) creating a second electrically conductive layer to overlie said first electrically conductive layer and the substrate, said second electrically conductive layer contacting the substrate in the unmasked region; and

e) chemical mechanical planarizing of a portion of said second electrically conductive layer to expose said first electrically conductive layer, a further portion of said second electrically conductive layer remaining in contact with the substrate.

16. The method as specified in Claim 15, further comprising the step of using silicon as said first and said second electrically conductive layers.

17. A method for forming an electrical interconnect, comprising the following steps:

a) creating a first electrically conductive layer overlying a substrate;

b) creating an etch stop layer overlying said first electrically conductive layer;

c) patterning said first electrically conductive layer and said etch stop layer to create a masked region and an unmasked region;

d) exposing the substrate in said unmasked region, thereby forming a via having a sidewall comprising said first electrically conductive layer and said etch stop layer;

e) creating a second electrically conductive layer to overlie said etch stop layer and the substrate, said second electrically conductive layer electrically contacting the substrate in the unmasked region; and

f) etching a portion of said second electrically conductive layer to expose said etch stop layer, at least a portion of said second electrically conductive layer remaining in electrical contact with the substrate to form a electrical plug of the electrical interconnect.

18. The method as specified in Claim 17, wherein the etch stop layer is a first etch stop layer and further comprising the following steps:

a) creating, overlying said first etch stop layer and the electrical contact, a layer which is capable of reacting with said second electrically conductive layer to form a layer which is irresponsive to an etchant which is capable of etching said second electrically conductive layer;

b) creating a reaction between said layer which is capable of reacting with said second electrically conductive layer and the electrical contact to form a second etch stop layer overlying the electrical contact, said first etch stop layer protecting said first electrically conductive layer from reacting with said layer which is capable of reacting with said second electrically conductive layer during said step of creating said reaction;

c) removing unreacted portions of said layer which is capable of reacting with said second electrically conductive layer;

d) removing at least portions of said first etch stop layer while retaining said second etch stop layer;

e) removing at least portions of said first electrically conductive layer, while retaining the electrical plug in its entirety during said steps (d and e) of

removing to form the electrical interconnect of the electrical plug and the remaining portion of the first electrically conductive layer.

19. The method as specified in Claim 17, further comprising the step of forming a protective layer overlying the electrical contact, said protective layer protecting the electrical contact during subsequent etching of said first electrically conductive layer.

20. The method as specified in Claim 17, further comprising the following steps:

a) depositing a titanium layer overlying said etch stop layer and the electrical contact; and

b) forming a layer of titanium silicide overlying the electrical contact.

21. The method as specified in Claim 20, further comprising the following steps:

a) removing at least portions of said first electrically conductive layer; and

b) retaining the electrical plug in its entirety during said step of removing.

22. The method as specified in Claim 17, further comprising the step of forming an oxide layer overlying the electrical contact.

23. The method as specified in Claim 22, further comprising the following steps:

a) removing at least portions of said first electrically conductive layer; and

b) retaining the electrical plug underlying said oxide layer during said step of removing.

24. The method as specified in Claim 17, wherein said step of exposing comprises the following steps:

a) etching said etch stop layer; and

b) etching the first electrically conductive layer.

25. The method as specified in Claim 17, further comprising using silicon as said first and said second electrically conductive layers.

26. A method for forming an electrical interconnect to a substrate, comprising the following steps:

a) depositing a first electrically conductive layer to overlie a substrate;

b) etching said first electrically conductive layer to form a via and expose a portion of the substrate at a bottom of the via;

c) depositing a second electrically conductive layer in said via to electrically contact the substrate and to overlie said first electrically conductive layer; and

d) removing said second electrically conductive layer overlying said first electrically conductive layer thereby eliminating a horizontal interface between said first and said second electrically conductive layers while retaining a portion of said second electrically conductive contacting the substrate.

27. The method as specified in Claim 26, further comprising using silicon as said first and said second electrically conductive layers.

28. A semiconductor interconnect for electrically connecting a first region of a substrate and a second region of the substrate, comprising:

a) an electrically conductive silicon plug overlying and in electrical contact with the first region and the second region; and

b) an electrically conductive silicon layer, without a silicon interface horizontal to the substrate, electrically isolated from the substrate and interposed between said silicon plug overlying the first region and said silicon plug overlying

the second region, wherein an interface between said silicon plug overlying the first region and said silicon layer is vertical to the substrate, and wherein an interface between said silicon plug overlying the second region and said silicon layer is vertical to the substrate.

29. A static random access memory device having an electrical interconnect for electrically connecting a first region of a substrate and a second region of the substrate, comprising:

a) an electrically conductive silicon plug overlying and in electrical contact with the first region and the second region; and

b) an electrically conductive silicon layer, without a silicon interface horizontal to the substrate, electrically isolated from the substrate and interposed between said silicon plug overlying the first region and said silicon plug overlying the second region, wherein an interface between said silicon plug overlying the first region and said silicon layer is vertical to the substrate, and wherein an interface between said silicon plug overlying the second region and said silicon layer is vertical to the substrate.

30. A dynamic random access memory device having an electrical interconnect for electrically connecting a first region of a substrate and a second region of the substrate, comprising:

a) an electrically conductive silicon plug overlying and in electrical contact with the first region and the second region; and

b) an electrically conductive silicon layer, without a silicon interface horizontal to the substrate, electrically isolated from the substrate and interposed between said silicon plug overlying the first region and said silicon plug overlying the second region, wherein an interface between said silicon plug overlying the first region and said silicon layer is vertical to the substrate, and wherein an interface between said silicon plug overlying the second region and said silicon layer is vertical to the substrate.

31. An electrical interconnect formed by the process, comprising the following steps:

a) creating a first electrically conductive layer overlying a substrate and having an opening therein exposing a portion of the substrate;

b) creating a second electrically conductive layer to overlie said first electrically conductive layer and the substrate, said second electrically conductive layer electrically contacting the substrate in the portion of the substrate which was exposed; and

c) removing said second electrically conductive layer from overlying said first electrically conductive layer, a portion of said second electrically conductive layer remaining in electrical contact with the portion of the substrate which was exposed.

32. A static random access memory device made by the process, comprising the following steps:

a) creating a first electrically conductive layer overlying a substrate and having an opening therein exposing a portion of the substrate;

b) creating a second electrically conductive layer to overlie said first electrically conductive layer and the substrate, said second electrically conductive layer electrically contacting the substrate in the portion of the substrate which was exposed; and

c) removing said second electrically conductive layer from overlying said first electrically conductive layer, a portion of said second electrically conductive layer remaining in electrical contact with the portion of the substrate which was exposed.

33. A dynamic random access memory formed by the process comprising, comprising the following steps:

a) creating a first electrically conductive layer overlying a substrate and having an opening therein exposing a portion of the substrate;

b) creating a second electrically conductive layer to overlie said first electrically conductive layer and the substrate, said second electrically conductive layer electrically contacting the substrate in the portion of the substrate which was exposed; and

c) removing said second electrically conductive layer from overlying said first electrically conductive layer, a portion of said second electrically conductive layer remaining in electrical contact with the portion of the substrate which was exposed.